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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,857	12/30/2003	Tim Allen	ALTRP108	6310

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

MAIL DATE	DELIVERY MODE
08/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,857	ALLEN, TIM	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-17,19-24 and 26-28* is/are rejected.

7)☒ Claim(s) *2,18 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

4. Claims 1, 3-17, 19-24 and 26-28 rejected under 35 U.S.C. 102(b) as being anticipated by Inaba et al. (Inaba), U.S. patent no. 4,396,987.

As per claim 1, Inaba discloses a system on a programmable chip [Numerical control device, fig. 3], the system comprising:

memory [col. 3, lines 13-16; col. 4, lines 17-22]; a processor [MPUN, fig. 3; col. 4, lines 22-23] couple to memory on the programmable chip, the processor operable to write streaming output information to memory [fig. 3; col. 4, lines 22-26];

a streaming output peripheral configured to generate clock cycle accurate output signals [pulses Xp and Zp; col. 4, lines 27-35], wherein the clock cycle accurate output signals are generated by reading streaming output information from memory and outputting signals based on the streaming output information [col. 3, lines 42-47; col. 5, lines 33-50].

As per claim 3, Inaba discloses streaming output information includes amplitude and timing information [col. 4, lines 27-37; col. 5, lines 33-50; col. 6, lines 29-35].

As per claim 4, Inaba discloses the streaming output information comprises a sequence of values written to memory [col. 5, lines 33-50].

As per claim 5, Inaba inherently discloses the sequence of values is associated with a periodic waveform [col. 5, lines 33-50].

As per claim 6, Inaba inherently discloses the sequence of values is associated with an event driven waveform [col. 4, lines 27-37; col. 5, lines 33-50; col. 6, lines 29-35].

As per claim 7, Inaba inherently discloses the sequence of values is associated with a scripted waveform [col. 4, lines 27-37; col. 5, lines 33-50; col. 6, lines 29-35].

As per claim 8, Inaba discloses the streaming output peripheral operates as a streaming parallel output [fig. 3; col. 4, lines 27-46].

As per claim 9, Inaba inherently discloses the streaming output peripheral operates as a digital to analog converter (DAC) [col. 5, lines 33-50].

As per claim 10, Inaba discloses the streaming output peripheral operates as a pulse width modulator [col. 9, lines 21-40].

As per claim 11, Inaba inherently discloses the clock cycle accurate output values are generated during expected clock cycles [col. 4, lines 27-35].

As per claim 12, Inaba inherently discloses the clock cycle accurate output values form clock cycle accurate waveforms [col. 4, lines 27-35].

As per claim 13, Inaba discloses the clock cycle accurate waveform is generated without intervention from the processor [col. 6, lines 29-50].

As per claim 14, Inaba discloses the streaming output peripheral receives address information from the processor indicating where to read streaming output information [col. 5, lines 35-50].

As per claim 15, Inaba discloses the address information comprises one or more memory addresses [col. 5, lines 35-50; col. 6, lines 29-50].

As per claim 16, Inaba discloses the memory, processor, and streaming output peripheral are connected using simultaneous multiple primary component fabric [fig. 3; col. 4, lines 17-30].

As to claims 17 and 19-23, Claims 1 and 3-16 basically are the corresponding elements that are carried out the method of operating steps in claims 17 and 19-23. Accordingly, claims 17 and 19-23 are rejected for the same reason as set forth in claims 1 and 3-16.

As per claims 24 and 26-28 are written in mean plus function and contained the same limitations as claims 1 and 3-16. Therefore, same rejection is applied.

Allowable Subject Matter

5. Claims 2, 18 and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Applicant's arguments filed 7/10/2007 have been fully considered but are not persuasive.

7. In the remarks, applicants argued in substance that in **Inaba** system, Inaba does

not mention on programmable chip or any clock cycles or clock cycle accurate output signals.

8. The examiner respectfully traverses. A programmable chip is a programmable integrated circuit as a device, such that Inaba discloses a programmable chip such as a numerical control device. Furthermore, Inaba discloses a streaming output peripheral configured to generate clock cycle accurate output signals [pulses Xp and Zp; col. 4, lines 27-35], as indicated in the claim language.

9. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aug. 14, 2007

CHUN CAO
PRIMARY EXAMINER